Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 YS**
2. **1 YP**
3. **1 STRB**
4. **1 RTC**
5. **1 B**
6. **1 RT**
7. **1 A**
8. **GND**
9. **2 A**
10. **2 RT**
11. **2 B**
12. **2 RTC**
13. **2 STRB**
14. **YP**
15. **YS**
16. **VCC**

**.060”**

**.060”**

**1 16 15**

**14**

**13**

**12**

**11**

**10**

**2**

**3**

**4**

**5**

**6**

**7 8 9**

**MASK**

**REF**

**75115B**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 75115B**

**APPROVED BY: DK DIE SIZE .060” X .060” DATE: 9/8/21**

**MFG: TEXAS INTRUMENTS THICKNESS .025” P/N: 55115**

**DG 10.1.2**

#### Rev B, 7/19/02